

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method for forming contact openings between bit line patterns, the method comprising the steps of:
 - a) forming bit line patterns on a substrate;
 - b) forming an interlayer insulating layer over the substrate;
 - c) etching the interlayer ~~insulting~~ insulating layer by using the bit line patterns and an etching mask defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns; and
 - d) forming spacers on sidewalls of the bit line patterns only exposed through the contact opening.
2. (Original) The method of claim 1, wherein the interlayer insulating layer is formed of a material having a dielectric constant less than 3.5.
3. (Original) The method of claim 2, wherein in step b), the interlayer insulating layer is formed of an oxide layer.

4. (Original) The method of claim 3, wherein in step c), the interlayer insulating layer is etched with a gas mixture including Ar, C, and F.

5. (Original) The method of claim 4, wherein in step c), the interlayer insulating layer is etched at a pressure of 1 mTorr to 100 mTorr.

6. (Currently Amended) [[A]]The method of claim 1, wherein top surfaces of the bit line patterns are covered with a layer selected from a group consisting of a silicon nitride layer, a silicon oxynitride layer, and an oxide layer.

7. (Original) The method of claim 2, wherein in step b), the interlayer insulating layer is formed of a polymer.

8. (Previously Presented) The method of claim 7, wherein in step c), the interlayer insulating layer is etched by using a gas selected from a group consisting of Ar, O₂, N₂, H₂, CH₄, C₂H₄, and C_xF_y.

9. (Original) The method of claim 8, wherein in step c), the interlayer insulating layer is etched at a pressure of 1 mTorr to 100 mTorr.

10-20. (Cancelled)